WHAT IS CLAIMED IS:

1. A semiconductor inspection method comprising steps of:

extracting adjacent lines which have a possibility of a short circuit occurring between the lines from a layout pattern of a semiconductor;

obtaining input logical values such that one of the adjacent lines has a logical value "1" while the other has a logical value "0"; and

monitoring an output of a logical circuit which receives the input logical values, and comparing the monitored output with an output logical value which is expected when the input logical values are input to the logical circuit.

2. A semiconductor inspection method comprising steps of:

extracting lines, a distance between said lines being equal to or less than a threshold, from layout data of a semiconductor as adjacent lines;

obtaining input logical values such that one of the adjacent lines has a logical value "1" while the other has a logical value "0"; and

monitoring an output of a logical circuit which receives the input logical values, and comparing the

monitored output with an output logical value which is expected when the input logical values are input to the logical circuit.

3. A computer-readable recording medium which records a program for making a computer execute steps of:

extracting adjacent lines which have a possibility of a short circuit occurring between the lines from a layout pattern of a semiconductor;

obtaining input logical values such that one of the adjacent lines has a logical value "1" while the other has a logical value "0"; and

monitoring an output of a logical circuit which receives the input logical values, and comparing the monitored output with an output logical value which is expected when the input logical values are input to the logical circuit.

4. A computer-readable recording medium which records a program for making a computer execute steps of:

extracting lines, a distance between said lines being equal to or less than a threshold, from layout data of a semiconductor as adjacent lines;

obtaining input logical values such that one of the adjacent lines has a logical value "1" while the other has

a logical value "0"; and

monitoring an output of a logical circuit which receives the input logical values, and comparing the monitored output with an output logical value which is expected when the input logical values are input to the logical circuit.